FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-24500-2E

ASSP

Single-chip Demodulator for Digital Satellite Broadcasting

MB86660A

■ DESCRIPTION

MB86660A is a single-chip demodulator for digital satellite broadcasting, and is compatible for DVB-S and DSS*. It consists of two A/D converters for I-input and Q-input, QPSK demodulator and forward-error correction (FEC) unit which has Viterbi decoder and Reed-Solomon decoder.

■ FEATURES

- DVB-S and DSS* compatible single-chip demodulator
- Operation rate up to 62 Mbps
- A/D converters for I-input and Q-input
  Analog 1 V p-p and up to 31 Msymbol/s input
- QPSK demodulator
  Gray-coded QPSK demodulation with absolute mapping
  On-chip multi-rate VCO (36 to 62 MHz operation)
  Automatic carrier capture range = ±5 MHz
  Half Nyquist filters roll-off factor $\alpha = 0.35$
  Automatic gain control (AGC): PWM output

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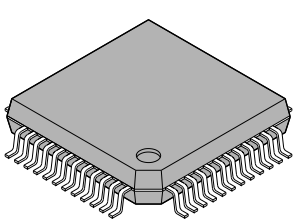
■ PACKAGE

48-pin plastic QFP



(FPT-48P-M15)

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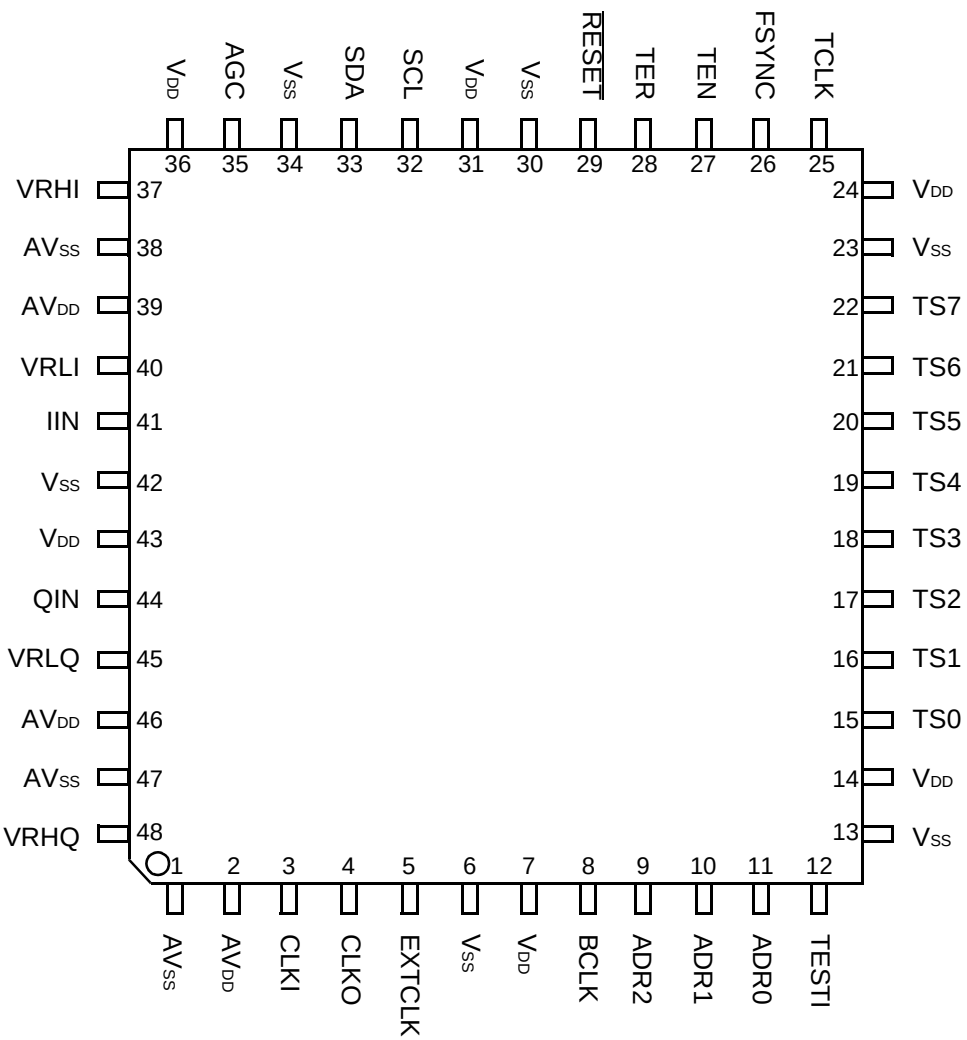
- Viterbi decoder
  Constraint length K = 7
  Viterbi rate R = 1/2, 2/3, 3/4, 5/6, 7/8
- Reed-Solomon decoder
  n = 204, k = 188, t = 8
- Deinterleaver: depth I = 12
- Energy-dispersal removal: PRBS polynomial = $x^{15} + x^{14} + 1$
- C/N monitoring output via I^2C interface
- I^2C bus interface
- Power supply voltage: +3.3 V
- Package: QFP-48
- Process: 0.35 µm CMOS

*****: For detailed information on DSS usage, please contact your nearest Fujitsu.

■ PIN ASSIGNMENT

< TOP VIEW >



(FPT-48P-M15)

■ PIN DESCRIPTION

Pin no.	Symbol	Pin name	I/O	Function
41	IIN	QPSK analog I-input	I	**QPSK analog in-phase input:** Analog 1 V p-p input. The maximum input rate is 31 Msymbol/s.
44	QIN	QPSK analog Q-input	I	**QPSK analog quadrature-phase input:** Analog 1 V p-p input. The maximum input rate is 31 Msymbol/s.
37	VRHI	A/D high reference	I	**A/D high reference input for IIN:** High reference voltage input. The typical voltage is 1.4 V.
40	VRLI	A/D low reference	I	**A/D low reference input for IIN:** Low reference voltage input. The typical voltage is 0 V.
48	VRHQ	A/D high reference	I	**A/D high reference input for QIN:** High reference voltage input. The typical voltage is 1.4 V.
45	VRLQ	A/D low reference	I	**A/D low reference input for QIN:** Low reference voltage input. The typical voltage is 0 V.
35	AGC	AGC output	O	**AGC output:** PWM (Pulse Width Modulation) or 'H/L' level output. This output pin is fed to an external analog filter that controls an AGC amplifier of the tuner.
3 4	CLKI CLKO	Crystal oscillator input	I I/O	**Crystal oscillator input:** Connect a 27.0 MHz crystal oscillator between these pins. It is used to set the frequency of internal multi-rate VCO. This crystal oscillator is not required when the EXTCLK pin inputs 27.0 MHz clock. When the crystal oscillator is not used, CLKI and CLKO must be 'L' and 'OPEN' respectively. When the crystal oscillator is used, EXTCLK must be 'L'.
5	EXTCLK	External clock input	I	**External clock input:** This pin inputs 27.0 MHz clock to set the frequency of internal multi-rate VCO. The crystal oscillator is not required when this pin is used. When this EXTCLK is not used, it must be 'L'.
22 to 15	TS7 to TS0	Transport packet data output	O	**Transport data output:** These pins are the transport stream packet data. User can select the output mode, either from 8-bit parallel data or serial data output. When parallel output, user can select MSB position, TS7 or TS0. When serial output, user can select the output pin position, TS0 or TS7. All selections are done by setting the register.
25	TCLK	Transport packet clock output	O	**Transport clock output:** This pin is the transport stream packet clock for TS7 to TS0. User can select the output mode that is parallel or serial clock, and select the clock polarity. All selections are done by setting the register.
27	TEN	Transport packet enable	O	**Transport enable output:** This pin outputs 'H' during the valid data of the packet, and outputs 'L' during the others such as the parity byte.

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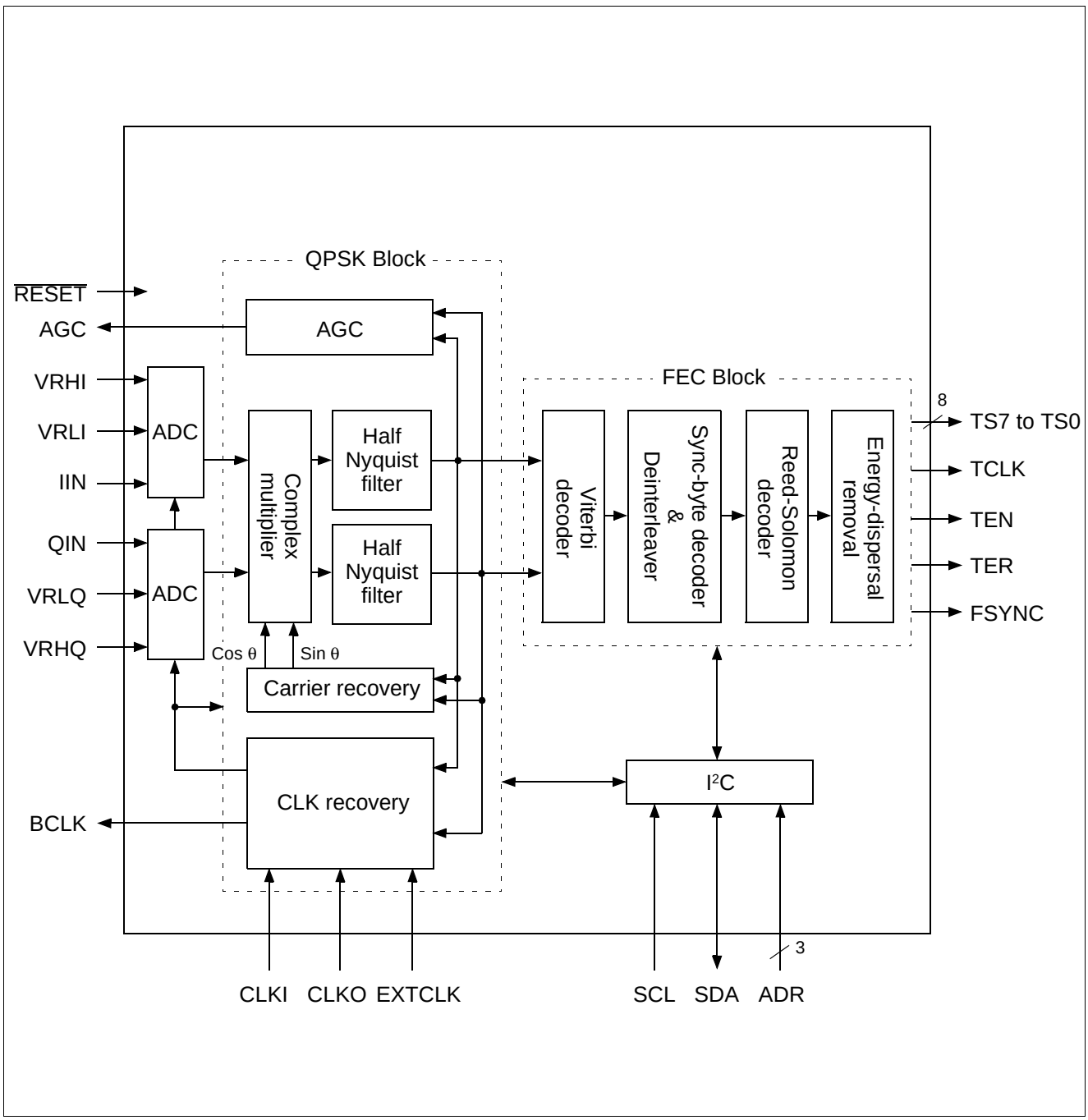
Pin no.	Symbol	Pin name	I/O	Function
28	TER	Error indicator	O	**Error indicator output:** This pin outputs 'H' for a period of a packet that the Reed-Solomon decoder could not correct, and outputs 'L' for a period of a packet that it could correct.
26	FSYNC	Frame synchronous output	O	**Frame synchronous output:** This pin outputs 'H' when the frame is synchronized.
32	SCL	I^2C bus clock	I	**Serial clock input for I^2C bus**
33	SDA	I^2C bus data	I/O	**Serial data I/O for I^2C bus**
9 10 11	ADR2 ADR1 ADR0	I^2C bus address	I	**Address ID input for I^2C bus:** These are the lower 3-bit of I^2C bus address. The upper 4-bit is fixed with "0001".
29	$\overline{\text{RESET}}$	Reset input	I	**Reset input:** The MB86660A is reset when this pin inputs 'L'. The LSI must be reset when the power is turned on. Refer to ■ Power-on Reset in detail.
8	BCLK	Bit clock output	O	**Bit clock output:** This pin can output the twice clock for the symbol rate, the same clock for the symbol rate, or the packet start signal. All selections are done by setting the register. This pin outputs 'L' at the initial stage.
12	TESTI	Test pin	I	**Test pin:** This input test pin must be connected to 'L'.
39, 46, 2	AV_{DD}	Analog V_{DD}	—	**Analog V_{DD}:** Analog V_{DD} for the internal A/Ds and VCO.
38, 47, 1	AV_{SS}	Analog V_{SS}	—	**Analog V_{SS}:** Analog GND for the internal A/Ds and VCO.
7, 14, 24, 31, 36, 43	V_{DD}	Digital V_{DD}	—	**Digital V_{DD}**
6, 13, 23, 30, 34, 42	V_{SS}	Digital V_{SS}	—	**Digital V_{SS}**

MB86660A

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	V_{DD}, AV_{DD}	–0.5	+4.0	V
Input voltage	V_I	–0.5	V_{DD} + 0.5	V
Output voltage	V_O	–0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	–55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{DD}, AV_{DD}	3.0	3.3	3.6	V
High level input voltage	V_{IH}	$V_{DD} \times 0.65$	—	V_{DD} + 0.3	V
Low level input voltage	V_{IL}	–0.3	—	$V_{DD} \times 0.25$	V
Operating temperature	Ta	0 to +70			°C

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = +3.3 ± 0.3 V, Ta = 0 to +70°C unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ. *1	Max.	
Logic input						
Input high voltage	V_{IH}	—	$V_{DD} \times 0.65$	—	V_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	—	$V_{DD} \times 0.25$	V
I^2C bus input (SDA and SCL)						
Input high voltage	V_{IH}	—	3.0	—	5.5	V
Input low voltage	V_{IL}	—	–0.5	—	1.5	V
A/D input (VRHI, VRHQ, VRLI, VRLQ, IIN and QIN)						
Input reference high voltage (for VRHI and VRHQ)	V_{RH}	—	V_{RL} + 1.0	1.4	V_{DD}	V
Input reference low voltage (for VRLI and VRLQ)	V_{RL}	—	0	0	V_{RH} – 1.0	V
Differential reference voltage	V_{RW}	$V_{RH} – V_{RL}$	1.0	1.4	2.5	V
Reference input resistance	R_{RW}	V_{RH} to V_{RL}	—	5	—	kΩ
Analog input voltage (for IIN and QIN)	V_i	—	V_{RL}	—	V_{RH}	V
Analog input capacitance (for IIN and QIN)	C_{in}	—	—	15	—	pF
Logic output						
Output high voltage	V_{OH}	I_{OH} = –4 mA	V_{DD} – 0.5	—	—	V
Output low voltage	V_{OL}	I_{OL} = 4 mA	—	—	0.4	V
I^2C bus output (SDA)						
Output low voltage	V_{OL}	I_{OL} = 3 mA	—	—	0.4	V
Power supply current (V_{DD} and AV_{DD})						
Average power supply current	I_{DD}	IIN, QIN = 31 Mbaud/s V_{DD} = 3.6 V	—	300	T.B.D.	mA

*1: Typical values assume that V_{DD} = +3.3 V and Ta = +25°C.

■ REGISTER TABLE

1. Register Map

<I²C address: | 0 | 0 | 0 | 1 | ADR2 | ADR1 | ADR0 | >

Register address	Access	Register name	(MSB) Bit function							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00000000 (0)	R/W	MODE-1	MOD7 (0)	Reserved (0)	MOD5 (0)	MOD4 (0)	MOD3 (0)	MOD2 (0)	MOD1 (0)	MOD0 (0)
00000001 (1)	R/W	MODE-2	Reserved (0)	Reserved (0)	Reserved (0)	BCLK1 (0)	BCLK0 (0)	ER_EN (1)	RS_EN (1)	DI_EN (1)
00000010 (2)	R/W	AGC	Reserved (0)	AGCP (0)	AGCM (0)	AGC4 (1)	AGC3 (0)	AGC2 (0)	AGC1 (0)	AGC0 (0)
00000011 (3)	R/W	VCO	VCO7 (0)	VCO6 (0)	VCO5 (0)	VCO4 (1)	VCO3 (0)	VCO2 (1)	VCO1 (1)	VCO0 (0)
00000100 (4)	R/W	Viterbi VCO Expansion	LVCO (0)	0	0	VIR4 (0)	VIR3 (0)	VIR2 (1)	VIR1 (0)	VIR0 (0)
00000101 (5)	R/W	Frame Sync.	SYT3 (1)	SYT2 (1)	SYT1 (1)	SYT0 (1)	SYA3 (0)	SYA2 (0)	SYA1 (1)	SYA0 (0)
00000110 (6)	R/W	Carrier Recovery loop filter Coeff.	CA_SW (1)	CA_β2 (0)	CA_β1 (1)	CA_β0 (0)	0	CA_α2 (0)	CA_α1 (0)	CA_α0 (1)
00000111 (7)	R/W	Clock Recovery loop filter Coeff.	0	CL_β2 (0)	CL_β1 (1)	CL_β0 (1)	0	CL_α2 (0)	CL_α1 (1)	CL_α0 (0)
00001000 (8)	W	RESET	X (0)	X (0)	X (0)	X (0)	X (0)	X (0)	QP_RST (0)	LSI_RST (0)
00001001 (9)	R	Status	X	X	X	STA4	STA3	STA2	STA1	STA0
00001010 (10)	R	AFC	AFC7	AFC6	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0
00001011 (11)	R	C/N	CN7	CN6	CN5	CN4	CN3	CN2	CN1	CN0
00001100 (12) • • • 00010000 (16)	— • • • —	Reserved • • • Reserved	X • • • X	X • • • X	X • • • X	X • • • X	X • • • X	X • • • X	X • • • X	X • • • X
00010001 (17)	R/W	Start Carrier Coeff.	X (0)	CAS_β2 (0)	CAS_β1 (1)	CAS_β0 (1)	X (0)	CAS_α2 (0)	CAS_α1 (1)	CAS_α0 (1)
00010010 (18)	R	Unused	1	1	1	1	1	1	1	1
00010011 (19)	R/W	AGC Coefficiency	X (0)	AGC_β2 (0)	AGC_β1 (0)	AGC_β0 (0)	X (0)	AGC_α2 (0)	AGC_α1 (1)	AGC_α0 (1)

Note: X: Don't care.
(0) or (1): Initial value

■ FUNCTIONAL DESCRIPTION

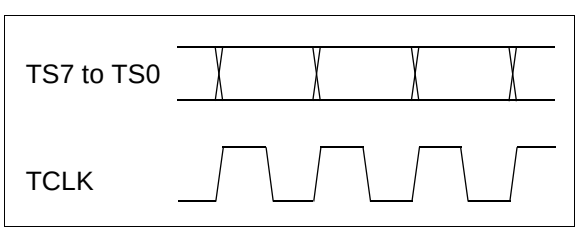
1. MODE-1

- User can select the output polarity of TCLK, the output mode of TS7 to TS0 and so on by setting the register.
- Register value: I^2C address = 0001ADR [2:0], Register address = 00000000 (2)

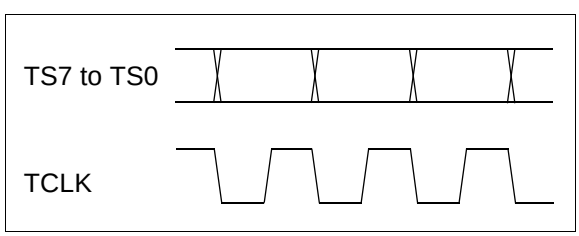
Bit name	Function	Bit value	Operation
MOD0	TCLK polarity	0 (initial)	TS7 to TS0 are latched at the falling edge of the TCLK.
		1	TS7 to TS0 are latched at the rising edge of the TCLK.
MOD1	Error indicator	0 (initial)	The error indicator flag of the transport stream packet is set to 'H' when the Reed-Solomon decoder cannot correct the error.
		1	The error indicator flag of the transport stream packet is not changed.
MOD2	Output mode of TS7 to TS0	0 (initial)	Parallel output.
		1	Serial output. Another TS bits output 'L'.
MOD3	Output order of TS7 to TS0	0 (initial)	TS7 is MSB when parallel. TS0 outputs when serial.
		1	TS0 is MSB when parallel. TS7 outputs when serial.
MOD4	FSYNC output mode	0 (initial)	FSYNC outputs the frame synchronous signal.
		1	FSYNC outputs the Viterbi synchronous signal.
MOD5	Frame sync-mode	0 (initial)	'B8(h)' of the frame sync-byte value is changed to '47(h)' inversely.
		1	'B8(h)' of the frame sync-byte value is not changed.
bit6	Reserved	0 (initial)	Don't change.
MOD7	Data reverse switch	0 (initial)	Normal operation.
		1	Received data is reversed in LSI.

[MOD0 function]

MOD0 = 0



MOD0 = 1



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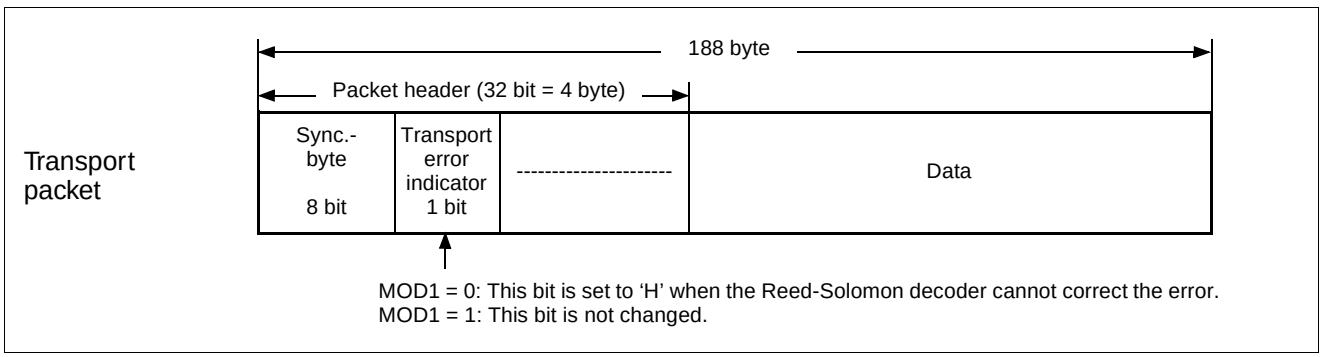
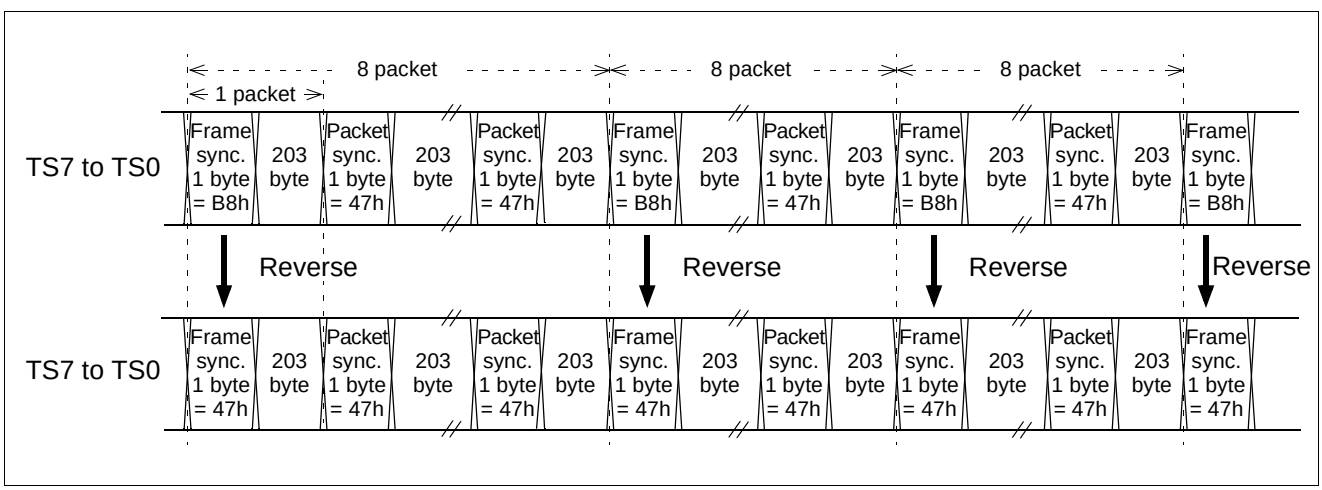
[MOD1 function]

The structure of the transport packet

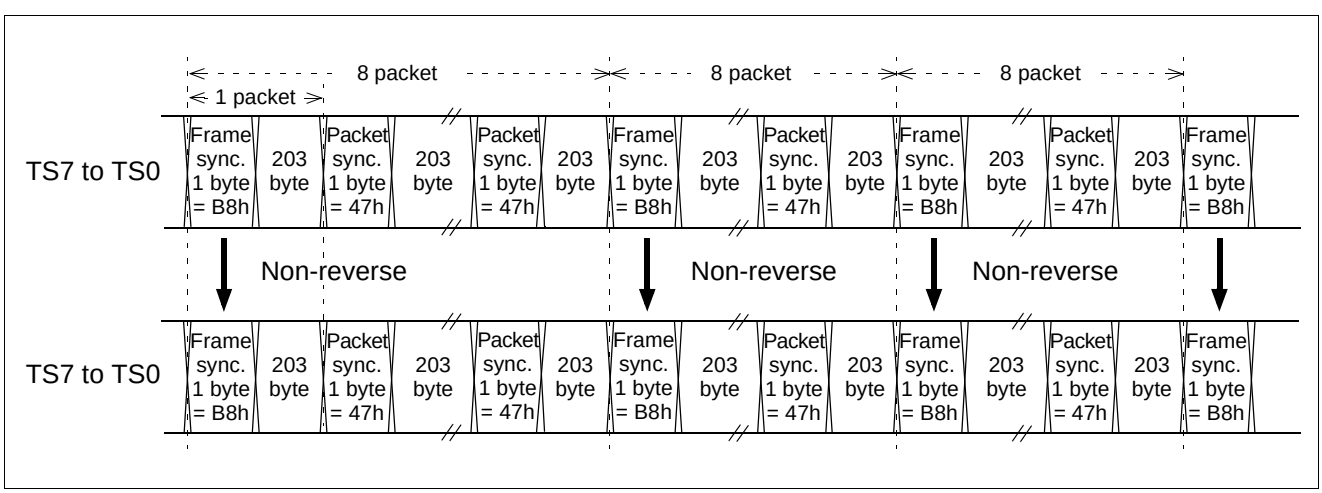


[MOD5 function]

MOD5 = 0



MOD5 = 1



2. MODE-2

- Deinterleaver, Reed-Solomon and Energy dispersal removal functions may be passed through by setting the register.
- Register value: I²C address = 0001ADR [2:0], Register address = 00000001 (2) = 1 (10)

Bit name	Function	Bit value	Operation
DI_EN	Deinterleaver enable	0	Deinterleaver is not performed.
		1 (initial)	Normal operation. Deinterleaver is performed.
RS_EN	Reed-Solomon enable	0	Read-Solomon decoder is not performed.
		1 (initial)	Normal operation. Reed-Solomon decoder is performed.
ER_EN	Energy dispersal removal enable	0	Energy dispersal removal is not performed.
		1 (initial)	Normal operation. Energy dispersal removal is performed.

- BCLK output may be changed by setting the register.
- Register value: I²C address = 0001ADR [2:0], Register address = 00000001 (2) = 1 (10)

Bit name	Function	Bit value	Operation
BCLK [1:0]	BCLK output select	00 (initial)	'L' level output.
		01	Packet start signal output.
		10	Clock of 2 × symbol rate is output.
		11	The same clock as symbol rate is output.

- It is prohibited to change the bit 5 to bit 7.
- Register value: I²C address = 0001ADR [2:0], Register address = 00000001 (2) = 1 (10)

Bit name	Function	Bit value	Operation
bit 5	Reserved	0 (initial)	Don't change.
bit 6		0 (initial)	Don't change.
bit 7		0 (initial)	Don't change.

3. Status

- User can monitor the internal status.
- Register value: I²C address = 0001ADR [2:0], Register address = 00001001 (2) = 9 (10), Read only

Bit name	Function	Bit value	Operation
STA0	Frame synchronization	0	It shows Frame isn't in synchronization.
		1	It shows Frame is in synchronization.
STA1	Viterbi decode synchronization	0	It shows the Viterbi decoder isn't in synchronization.
		1	It shows the Viterbi decoder is in synchronization.
STA [4:2]	Viterbi rate detection	000	It shows the Viterbi decoder isn't in synchronization.
		001	It shows the Viterbi rate is 1/2.
		010	It shows the Viterbi rate is 2/3.
		011	It shows the Viterbi rate is 3/4.
		100	It shows the Viterbi rate is 5/6.
		101	It shows the Viterbi rate is 7/8.

4. A/D converter

- I and Q analog input data are automatically sampled by the internal clock.

5. Nyquist filter

- Digital half Nyquist filtering is done for each I and Q input signal. The roll-off factor is 0.35.

6. AGC

- The amplitude of I and Q input data is compared with the reference value AGC [4:0] set by the register. The compared result is output to AGC pin by the PWM (Pulse Width Modulation) form or 'H/L' level. It adjusts the amplifier gain of the tuner via the external analog filter.
- The pulse width of the PWM output is changed at 1/(2Fs) × n (μs) step (n=0 to 255, Fs: symbol rate (Msymbol/s)). The frequency is Fs/128 (MHz).
- The pulse width of the 'H/L' level output is changed at minimum 4/Fs (μs) step (Fs: symbol rate (Msymbol/s)). The frequency is maximum Fs/4 (MHz). As the response is rapider than PWM, it is useful to a quick response request.
- The reference value AGC [4:0] and the AGC output polarity are programmable.
- Register value: I^2C address = 0001ADR [2:0], Register address = $00000010_{(2)} = 2_{(10)}$

Bit name	Function	Bit value	Operation
AGC [4:0]	Reference value for AGC	00000	Minimum reference value.
		to	
		10000 (initial)	The amplifier gain of the tuner is adjusted to equal to the reference value.
		to	
		11111	Maximum reference value.
AGCM	AGC output mode	0 (initial)	PWM output.
		1	'H/L' level output.
AGCP	AGC output polarity	0 (initial)	When AGC [4:0] > Amplitude of I and Q input data: • When AGCM = 0 (PWM output), it repeatedly outputs the pulse that 'H' period is longer than 'L' period. • When AGCM = 1 ('H/L' level output), it outputs 'H'. When AGC [4:0] < Amplitude of I and Q input data: • When AGCM = 0 (PWM output), it repeatedly outputs the pulse that 'L' period is longer than 'H' period. • When AGCM = 1 ('H/L' level output), it outputs 'L'.
		1	When AGC [4:0] > Amplitude of I and Q input data: • When AGCM = 0 (PWM output), it repeatedly outputs the pulse that 'L' period is longer than 'H' period. • When AGCM = 1 ('H/L' level output), it outputs 'L'. When AGC [4:0] < Amplitude of I and Q input data: • When AGCM = 0 (PWM output), it repeatedly outputs the pulse that 'H' period is longer than 'L' period. • When AGCM = 1 ('H/L' level output), it outputs 'H'.
bit 7	Reserved	0 (initial)	• Do not set this bit.

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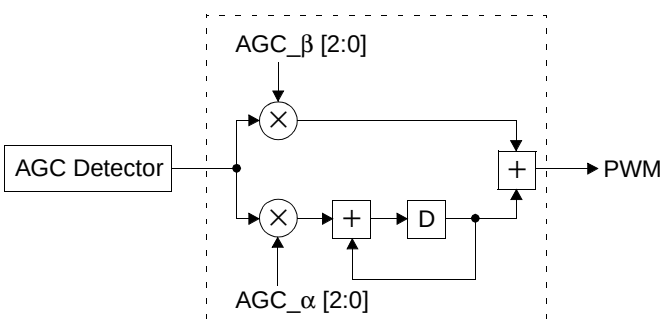
- Some external AGC-loop configuration in user systems may need to adjust the filter value using the following register.
- Register value: I²C address = 0001ADR [2:0], Register address = 00010011 (2) = 19 (10)

Bit name	Function	Bit value	Operation
AGC_α [2:0]	α-Coefficiency of AGC loop-filter	000	$\alpha = 2^0$ (= 1)
		001	$\alpha = 2^1$ (= 2)
		010	$\alpha = 2^2$ (= 4)
		011 (default)	$\alpha = 2^3$ (= 8)
		100	$\alpha = 2^4$ (= 16)
		101	$\alpha = 2^5$ (= 32)
		110	$\alpha = 2^6$ (= 64)
		111	—
AGC_β [2:0]	β-Coefficiency of AGC loop-filter	000 (default)	β = 0
		001	$\beta = 2^1$ (= 2)
		010	$\beta = 2^2$ (= 4)
		011	$\beta = 2^3$ (= 8)
		100	$\beta = 2^4$ (= 16)
		101	$\beta = 2^5$ (= 32)
		110	$\beta = 2^6$ (= 64)
		111	$\beta = 2^7$ (= 128)

Block Diagram of AGC:



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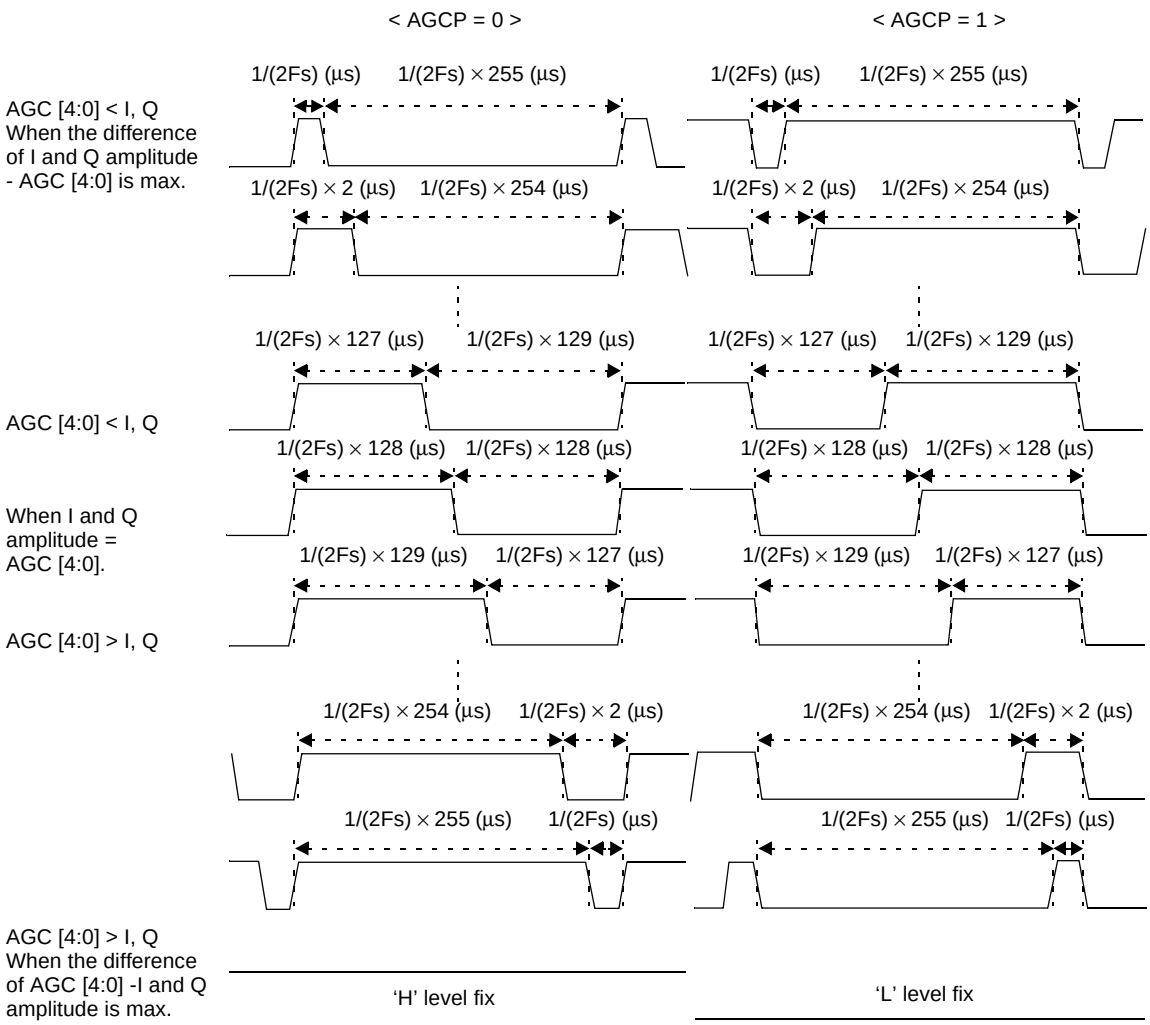
PWM AGC output wave form: The pulse width is changed at 1/(2Fs) × n (µs) step (n = 0 to 255, Fs: symbol rate (Msymbol/s).
The frequency is Fs/128 (MHz).



* Fs: symbol rate (Msymbol/s)

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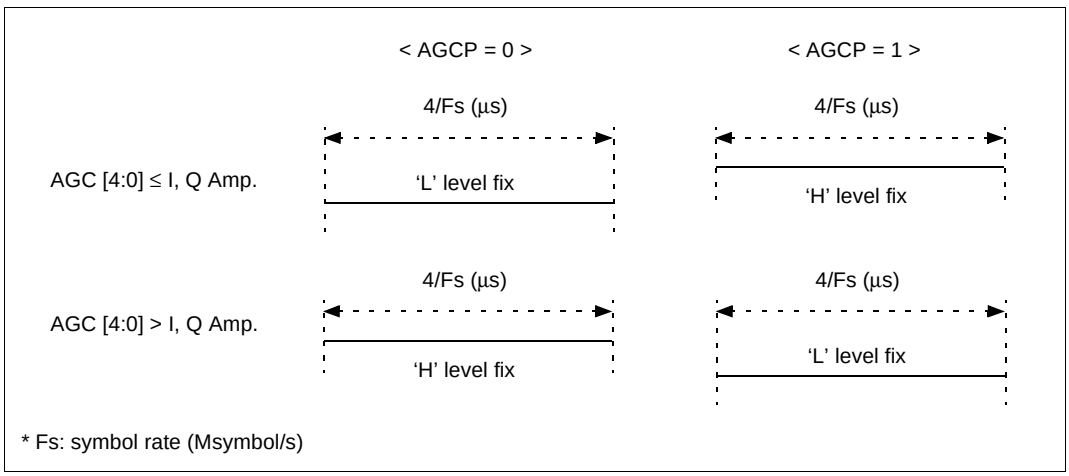
'H/L' level AGC output wave form: The pulse width is changed at minimum 4/Fs (µs) step (Fs: symbol rate)
The frequency is Fs/8 (MHz)



7. Carrier recovery

- The difference of the carrier recovery in the tuner is automatically recovered up to ±5 MHz in the LSI.
- The loop filter coefficient for the carrier recovery operates with CAS_α [2:0] and CAS_β [2:0] at first and then automatically switches to CA_α [2:0] and CA_β [2:0] after the lock-up. However, when CA_SW is “0”, the filter coefficient always operates with CA_α [2:0] and CA_β [2:0].
- The loop filter is variable.
- Register value: I²C address = 0001ADR [2:0]

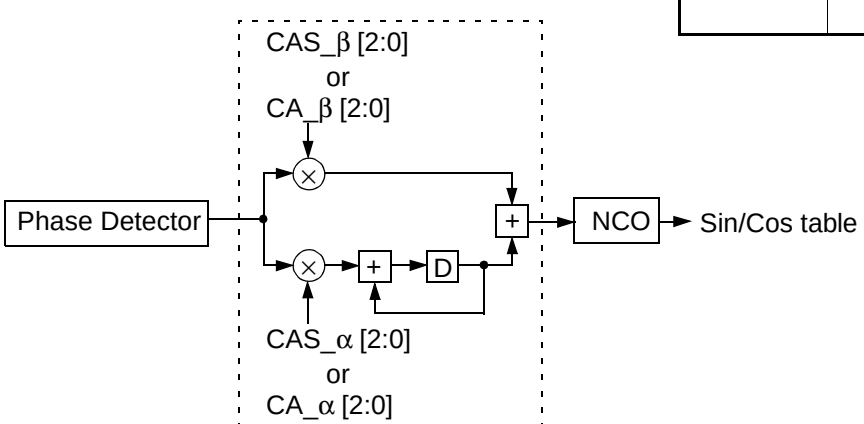
<Register address = 00010001(2) = 17(10)>

Bit name	Function	Bit value	Operation
CAS_α [2:0]	α-factor for the loop filter at first	000	$\alpha = 2^1$ (=2)
		001	$\alpha = 2^2$ (=4)
		010	$\alpha = 2^3$ (=8)
		011 (initial)	$\alpha = 2^4$ (=16)
		100	$\alpha = 2^5$ (=32)
		101 to 111	$\alpha = 2^6$ (=64)
CAS_β [2:0]	β-factor for the loop filter at first	000	$\beta = 2^8$ (=256)
		001	$\beta = 2^9$ (=512)
		010	$\beta = 2^{10}$ (=1024)
		011 (initial)	$\beta = 2^{11}$ (=2048)
		100	$\beta = 2^{12}$ (=4096)
		101 to 111	$\beta = 2^{13}$ (=8192)

<Register address = 00000110(2) = 6(10)>

Bit name	Function	Bit value	Operation
CA_α [2:0]	α-factor for the loop filter after lock-up	000	$\alpha = 2^1$ (=2)
		001 (initial)	$\alpha = 2^2$ (=4)
		010	$\alpha = 2^3$ (=8)
		011	$\alpha = 2^4$ (=16)
		100	$\alpha = 2^5$ (=32)
		101 to 111	$\alpha = 2^6$ (=64)
CA_β [2:0]	β-factor for the loop filter after lock-up	000	$\beta = 2^8$ (=256)
		001	$\beta = 2^9$ (=512)
		010 (initial)	$\beta = 2^{10}$ (=1024)
		011	$\beta = 2^{11}$ (=2048)
		100	$\beta = 2^{12}$ (=4096)
		101	$\beta = 2^{13}$ (=8192)
CA_SW	Loop filter SW	0	Auto SW: off
		1(initial)	Auto SW: on

Carrier Recovery Block Diagram:



8. AFC

- User can monitor the difference of the local oscillator frequency in the tuner.
- The different frequency of the tuner may be calculated by the following way by reading the register of AFC [7:0].

  Δf (KHz) = (128 – AFC [7:0]) $\times$ 82.474 $\times$ (n/42.192) (n: Receiving bit rate (Mbps))

  Ex.1: When AFC [7:0] = 01111100 and Receiving bit rate n = 40 (Mbps),

  AFC $_{(DEC)} = 2^2 + 2^3 + 2^4 + 2^5 + 2^6 = 124$

  Δf = 312.8 (KHz) $\rightarrow$ It shows the local oscillator frequency in the tuner is 312.8KHz higher.

  Ex.2: When AFC [7:0] = 10000101 and Receiving bit rate n = 60 (Mbps),

  AFC $_{(DEC)} = 2^0 + 2^2 + 2^7 = 133$

  Δf= –586.4(KHz) $\rightarrow$ It shows the local oscillator frequency in the tuner is 586.4KHz lower.
- Register value: I^2C address = 0001ADR [2:0], Register address = 00001010 $_{(2)}$, Read only

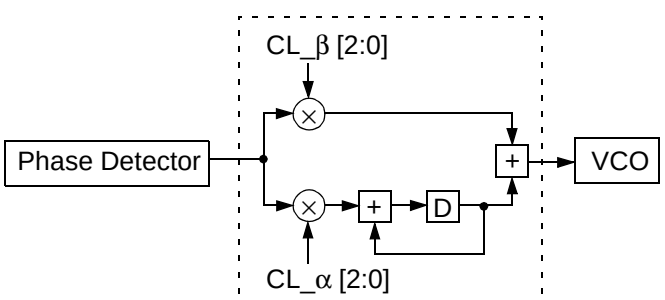
Bit name	Function	Bit value	Operation
AFC [7:0]	The difference of the carrier frequency	00000000	It shows the local oscillator frequency in the tuner is very high.
		00000001	
		to	
		01111111	
		10000000	It shows the local oscillator frequency in the tuner is almost fit.
		10000001	
		to	
		11111110	
		11111111	It shows the local oscillator frequency in the tuner is very low.

9. Clock recovery

- The clock synchronized to the base band data is automatically recovered in the LSI. The internal VCO must be set to the required frequency in advance. Refer to '10. VCO' for setting the internal VCO frequency.
- The Loop filter is variable.
- Register value: I^2C address = 0001ADR [2:0], Register address = $00000111_{(2)} = 7_{(10)}$

Bit name	Function	Bit value	Operation
CL_α [2:0]	α-factor for the clock recovery loop filter	000	$\alpha = 2^9$ (=512)
		001	$\alpha = 2^{10}$ (=1024)
		010 (initial)	$\alpha = 2^{11}$ (=2048)
		011	$\alpha = 2^{12}$ (=4096)
		100	$\alpha = 2^{13}$ (=8192)
		101	$\alpha = 2^{14}$ (=16384)
		110, 111	Prohibited
CL_β [2:0]	β-factor for the clock recovery loop filter	000	$\beta = 2^{17}$ (=131072)
		001	$\beta = 2^{18}$ (=262144)
		010	$\beta = 2^{19}$ (=524288)
		011 (initial)	$\beta = 2^{20}$ (=1048576)
		100	$\beta = 2^{21}$ (=2097152)
		101	$\beta = 2^{22}$ (=4194304)
		110, 111	Prohibited

Clock Recovery Block Diagram:



10. VCO

- The internal VCO frequency must be set to two times of the received data symbol rate. Because the frequency step is every 0.1 MHz step, set the nearest frequency.
  E.X.: When the received data symbol rate is 21.096 Msym/s, set 42.2 MHz as 21.096 Msym/s x2 = 42.192 MHz
- Register value: I^2C adress = 0001ADR [2:0], Register address = $00000011_{(2)} = 3_{(10)}$ & $00000100_{(2)} = 4_{(10)}$

Bit name	Function	Bit value	Operation	
			LVCO register = '0'	LVCO register = '1'
VCO [7:0]	VCO Freq. (0.1 MHz step)	00000000	Internal VCO is set to **40.0 MHz**.	
		00000001	Internal VCO is set to **40.1 MHz**.	
		to	to	
		00000110	Internal VCO is set to **40.6 MHz**.	
		to	to	
		00010110	Internal VCO is set to **42.2 MHz**. **(Initial value)**	
		to	to	
		01000100	Internal VCO is set to **46.8 MHz**.	
		to	to	
		01110100	Internal VCO is set to **51.6 MHz**.	
		to	to	
		10010110	Internal VCO is set to **55.0 MHz**.	
		to	to	
		10100010	Internal VCO is set to **56.2 MHz**.	
		to	to	
		11001000	Internal VCO is set to **60.0 MHz**.	
		to	to	
		11011000	Internal VCO is set to **61.6 MHz**.	Set to 36.0 MHz
		to	to	to
		11100000	Internal VCO is set to **62.4 MHz**.	Set to 36.8 MHz
		to	to	to
		11111110	Internal VCO is set to **65.4 MHz**.	Set to 39.8 MHz
		11111111	Internal VCO is set to **65.5 MHz**.	Set to 39.9 MHz

11. RESET

- The whole block of LSI or QPSK-Block only is reset when LSI_RST or QP_RST bit is set to ‘1’.
- Register value: I^2C address = 0001ADR [2:0], Register address = 00001000 (2) = 8(10)

Bit name	Function	Bit value	Operation
LSI_RST	The whole of LSI Software reset	1	The whole of LSI is reset when LSI_RST bit is set to ‘1’.
QP_RST	QPSK Block Software reset	1	QPSK-Block only is reset when QP_RST bit is set to ‘1’.

12. Viterbi decoder

- Constraint length K = 7.
- Optionally some Viterbi rates may be selected from R = 1/2, 2/3, 3/4, 5/6 and 7/8.
- The receiving Viterbi rate is automatically detected from some selected Viterbi rates. It is getting longer to detect it in proportion to the number of selected rates. So it is recommended to select one rate, if the rate is known beforehand.
- The detected Viterbi rate is written to the STA [4:2] register which is shown in ‘3. Status’.
- Register value: I^2C address = 0001ADR [2:0], Register address = 00000100 (2) = 4(10)

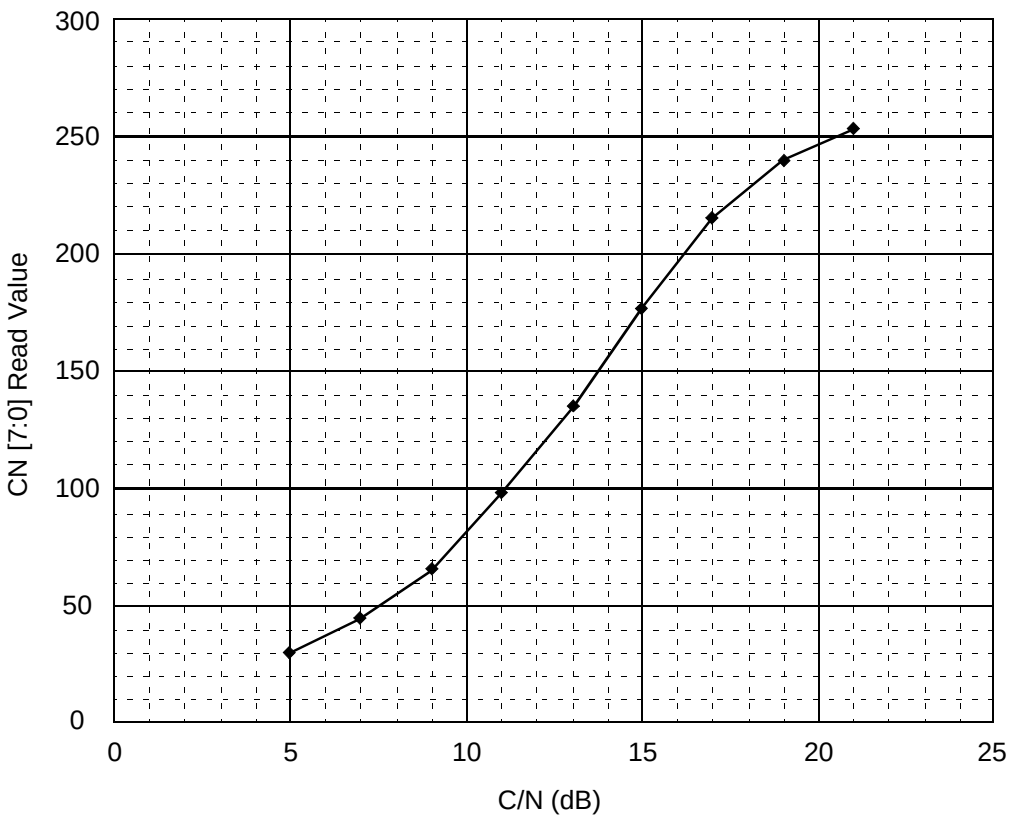
Bit name	Function	Bit value	Operation
VIR0	R = 1/2 setting	0 (initial)	Viterbi rate detection is not performed for R = 1/2.
		1	Viterbi rate detection is performed for R = 1/2.
VIR1	R = 2/3 setting	0 (initial)	Viterbi rate detection is not performed for R = 2/3.
		1	Viterbi rate detection is performed for R = 2/3.
VIR2	R = 3/4 setting	0	Viterbi rate detection is not performed for R = 3/4.
		1 (initial)	Viterbi rate detection is performed for R = 3/4.
VIR3	R = 5/6 setting	0 (initial)	Viterbi rate detection is not performed for R = 5/6.
		1	Viterbi rate detection is performed for R = 5/6.
VIR4	R = 7/8 setting	0 (initial)	Viterbi rate detection is not performed for R = 7/8.
		1	Viterbi rate detection is performed for R = 7/8.

13. C/N monitor

- The approximate C/N value of the LSI input is monitored.
- The monitored C/N value depends on evaluation circumstance, LSI mounting conditions, and so on in user application system. Therefore, the value must be carefully checked before user's finished product. The typical characteristic curve is shown in below.
- Register value: I^2C address = 0001ADR [2:0], Register address = $00001011_{(2)} = 11_{(10)}$, Read only

Bit name	Function	Bit value	Operation
CN [7:0]	C/N monitor	00000000	It shows the error of the receiving data is large.
		to	
		11111111	It shows the error of the receiving data is small.

C/N Monitor Characteristics



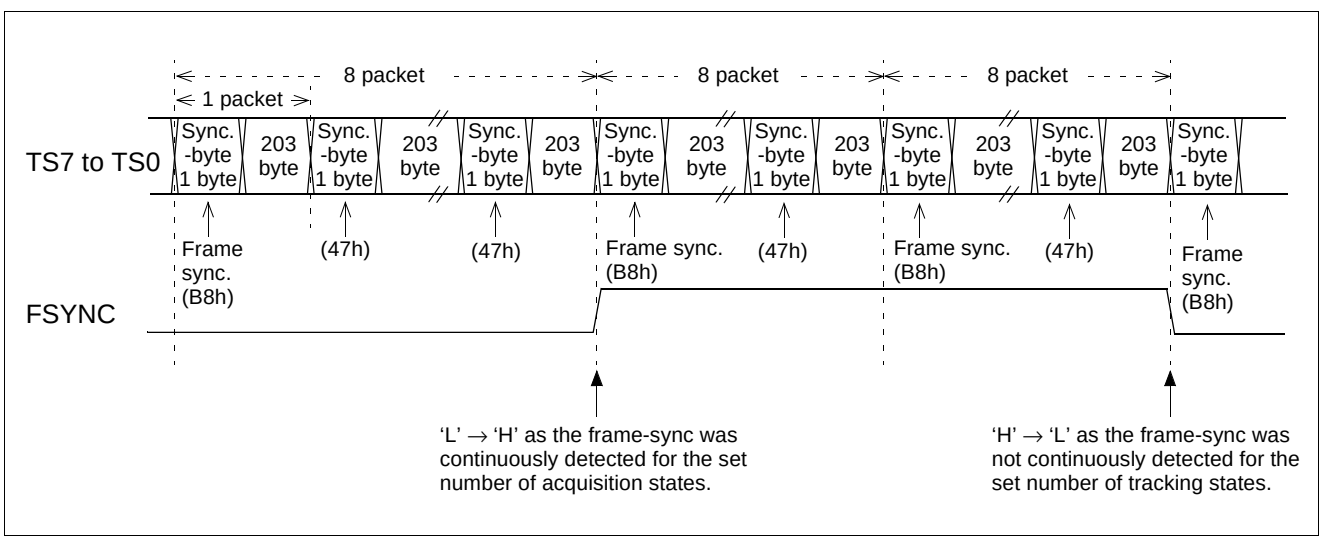
Note: CN [7:0] Read Value is transferred to the decimal value.

14. Frame synchronization

- The frame synchronization signal (B8h) on the head of 8 packets is detected. The number of states for acquisition and tracking is programmable.
- The LSI is judged to lock if the synchronization signal would be continuously detected for the set number of acquisition states, and then FSYNC is changing to 'H' (when MOD4 (Register address: 00000000) = '0'). After lock, the LSI is judged not to lock if the synchronization signal would not be continuously detected for the set number of tracking states, and then FSYNC is changing to 'L'.
- Register value: I^2C address = 0001ADR [2:0], Register address = 00000101 $_{(2)}$ = 5$_{(10)}$

Bit name	Function	Bit value	Operation
SYA [3:0]	Number of acquisition states	0000,0001, 0010 (initial)	The LSI is judged to lock if the synchronization signal would be continuously detected two times.
		to	
		1111	The LSI is judged to lock if the synchronization signal would be continuously detected fifteen times.
SYT [3:0]	Number of tracking states	0000 to 0010	The LSI is judged not to lock if the synchronization signal would not be continuously detected two times.
		to	
		1111 (initial)	The LSI is judged not to lock if the synchronization signal would not be continuously detected fifteen times.

Timing



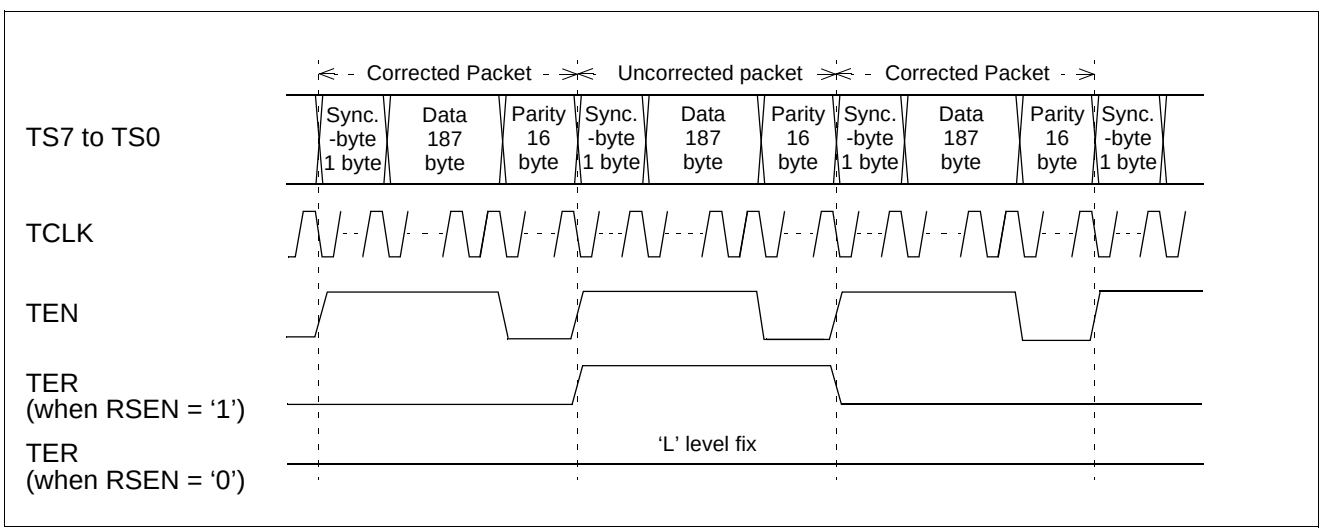
15. Deinterleaver

- The deinterleaving depth I = 12 on byte-stream.
- When DI_EN (Register address =00000001) = '0', Deinterleaver is not performed.
  When DI_EN = '1', Deinterleaver is performed.

16. Reed-Solomon decoder

- n = 204, k = 188, t = 8
  Code Generator Polynomial: $g(x) = (x + \lambda^0)(x + \lambda^1)(x + \lambda^2) \cdots (x + \lambda^{15})$
  Field Generator Polynomial: $p(x) = x^8 + x^4 + x^3 + x^2 + 1$
- If the total errors are less than 8 bytes at 204 bytes unit, all errors can be corrected. If the total errors are more than 9 bytes, all errors are not corrected. The TER outputs 'L' for a packet that all errors were corrected. The TER outputs 'H' for a packet that the errors were not corrected.
- To distinguish the parity bytes of Reed-Solomon, the TEN outputs 'H' for a period of the valid data, and then outputs 'L' for a period of the parity bytes.
- When RS_EN (Register address: 00000001) = '0', Reed-Solomon decoder is not performed and all errors are not corrected. TEN operates normally, but TER outputs 'L'.
  When RS_EN = '1', Reed-Solomon decoder is performed.

Timing

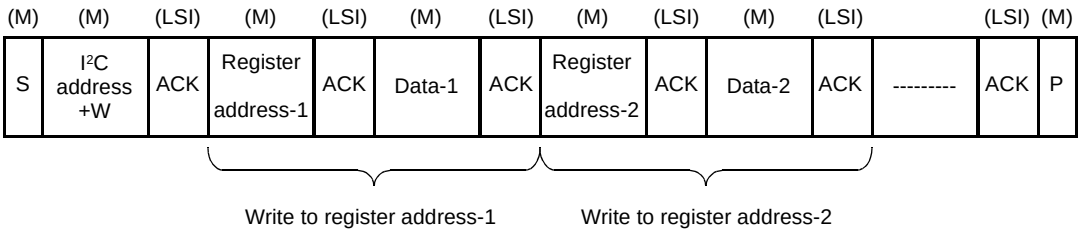


17. Energy dispersal removal

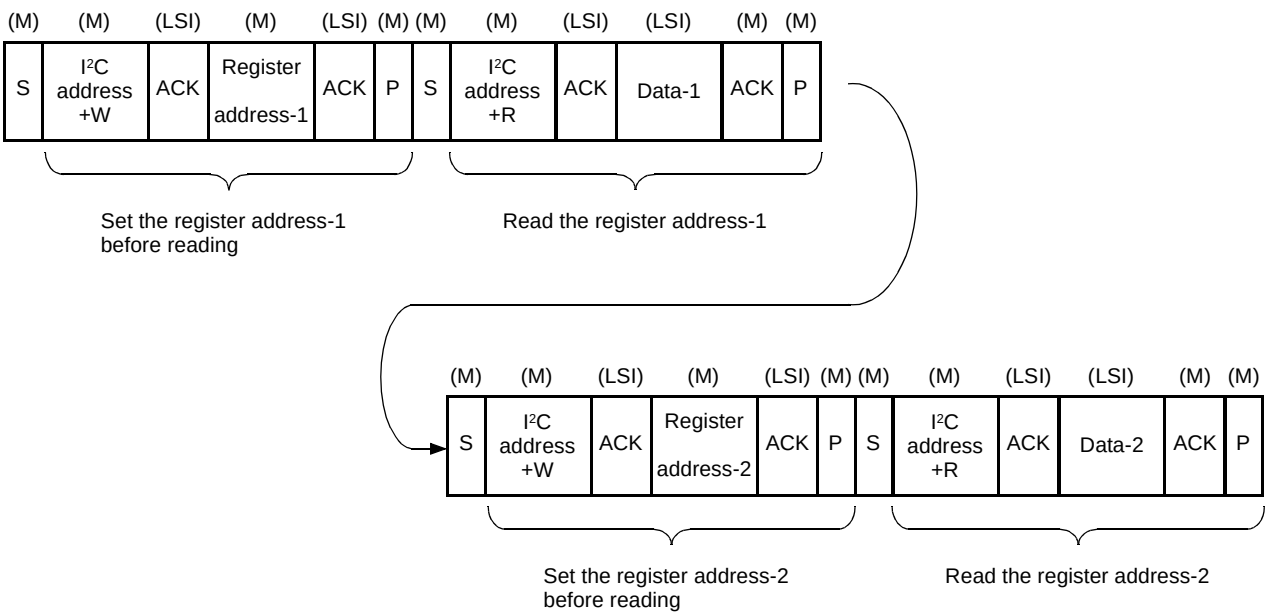
- When ER_EN (Register address: 00000001) = '0', Energy dispersal removal is not performed.
  When ER_EN = '1', Energy dispersal removal is performed.
- Pseudo Random Binary Sequence (PRBS) Polynomial: $x^{15} + x^{14} + 1$
  The polynomial is initialized into the sequence '100101010000000' every eight packets.

18. I²C bus

- Write format

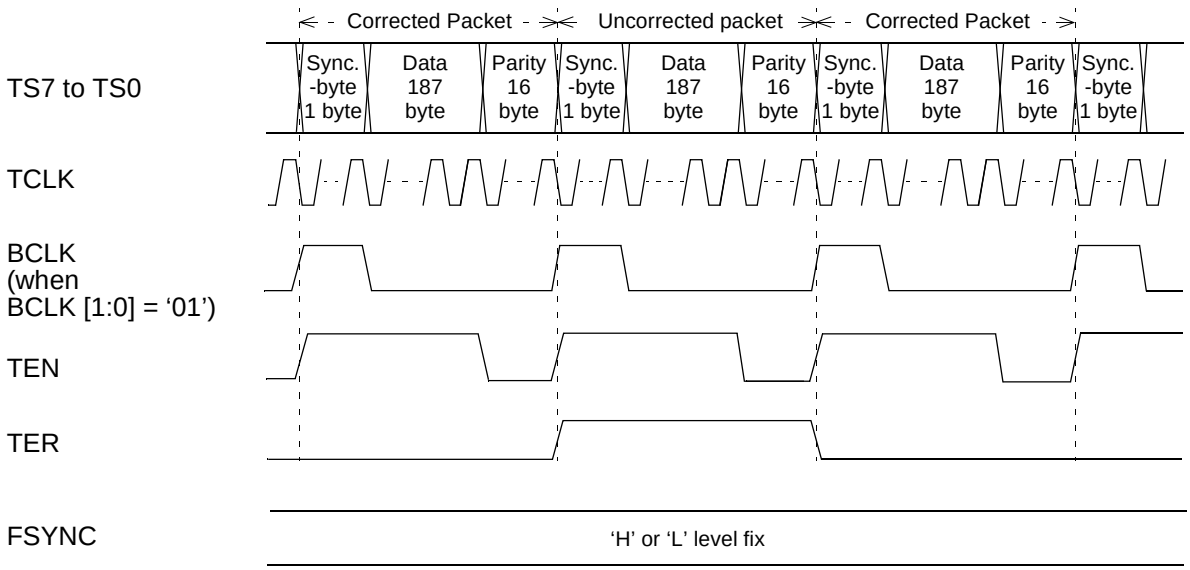


- Read format



Note: S: Start condition
I²C address (7bit): 0001 (ADR2) (ADR1) (ADR0)
ADR [2:0]: user setting
R/W (1bit): 0 = write, 1 = read
Data-n (8bit): Data of register address-n
ACK: Acknowledge
P: Stop condition
(M) : Output signal of I²C master
(LSI): Output signal of MB86660A

■ OUTPUT SIGNAL TIMING

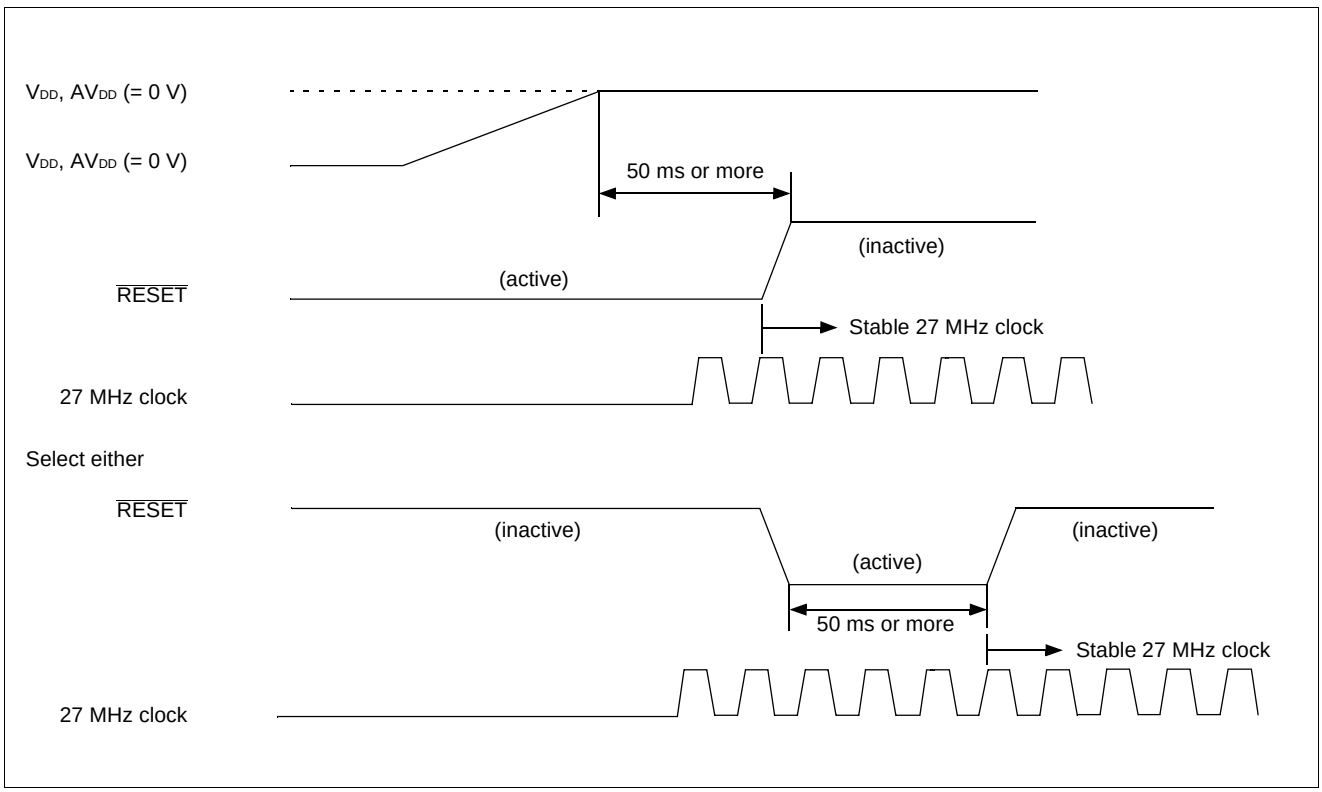


Note: TCLK polarity may be changed by setting the register.

■ POWER-ON RESET

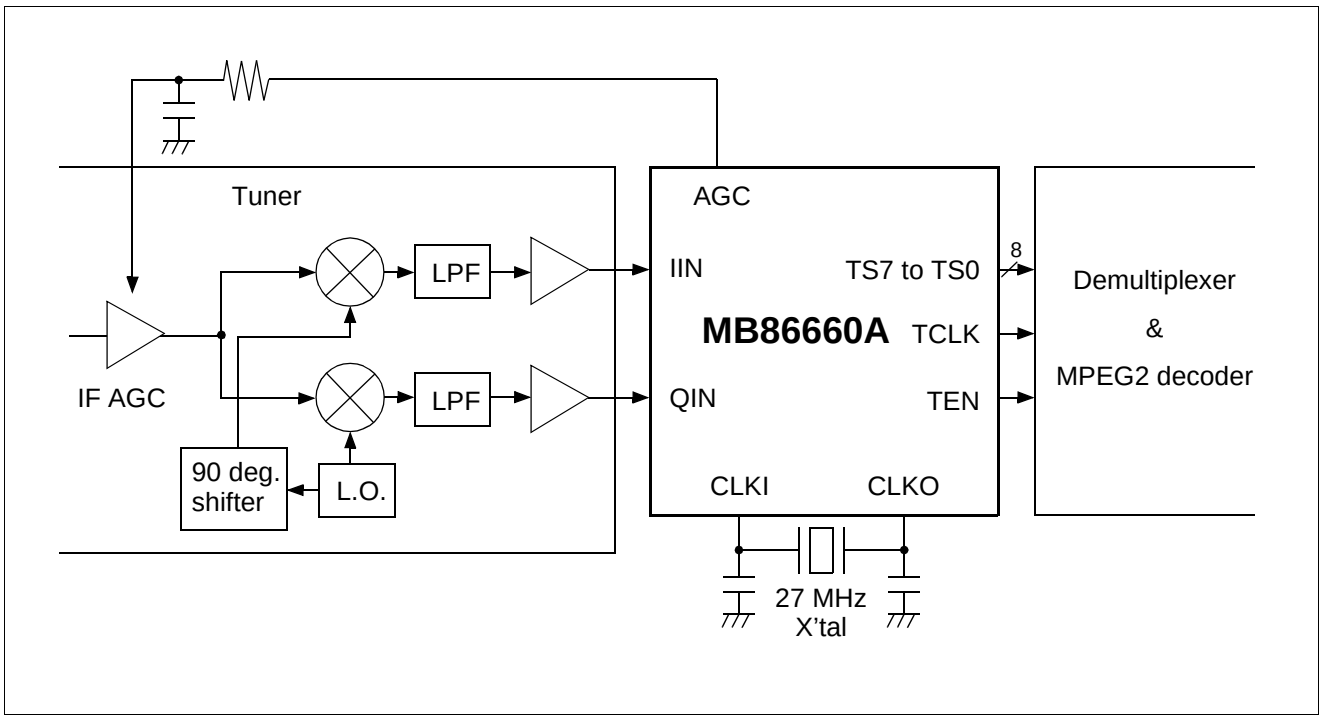
The MB86660A must be reset via $\overline{\text{RESET}}$ pin when the power is turned on.

- Apply a reset signal to the LSI at power-on, then cancel the reset 50 ms after the V_{DD} and AV_{DD} have reached 3.3 V or input a reset pulse with a width of 50 ms after they reached 3.3 V. Note that the 27.0 MHz clock by the crystal oscillator or the external clock of EXTCLK must be stable before the reset is canceled. (See the diagram below.)

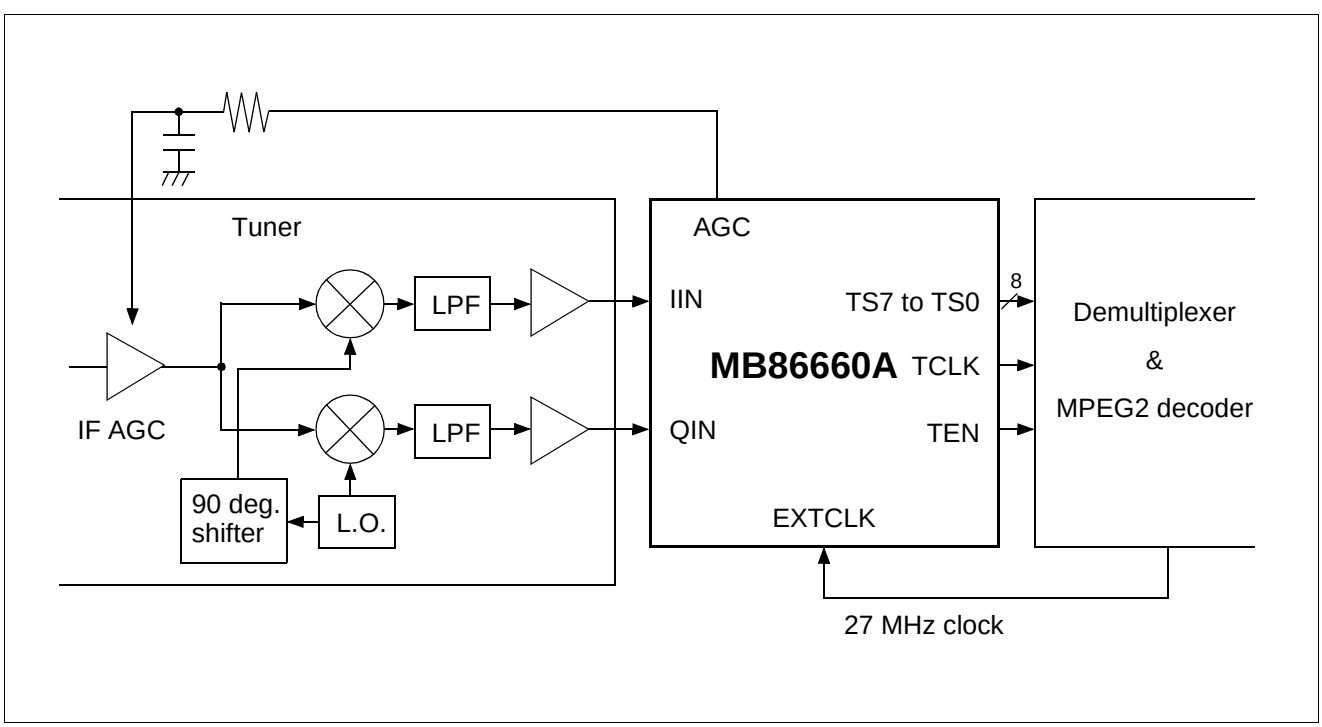


■ APPLICATION EXAMPLE

- When 27 MHz crystal oscillator is used.

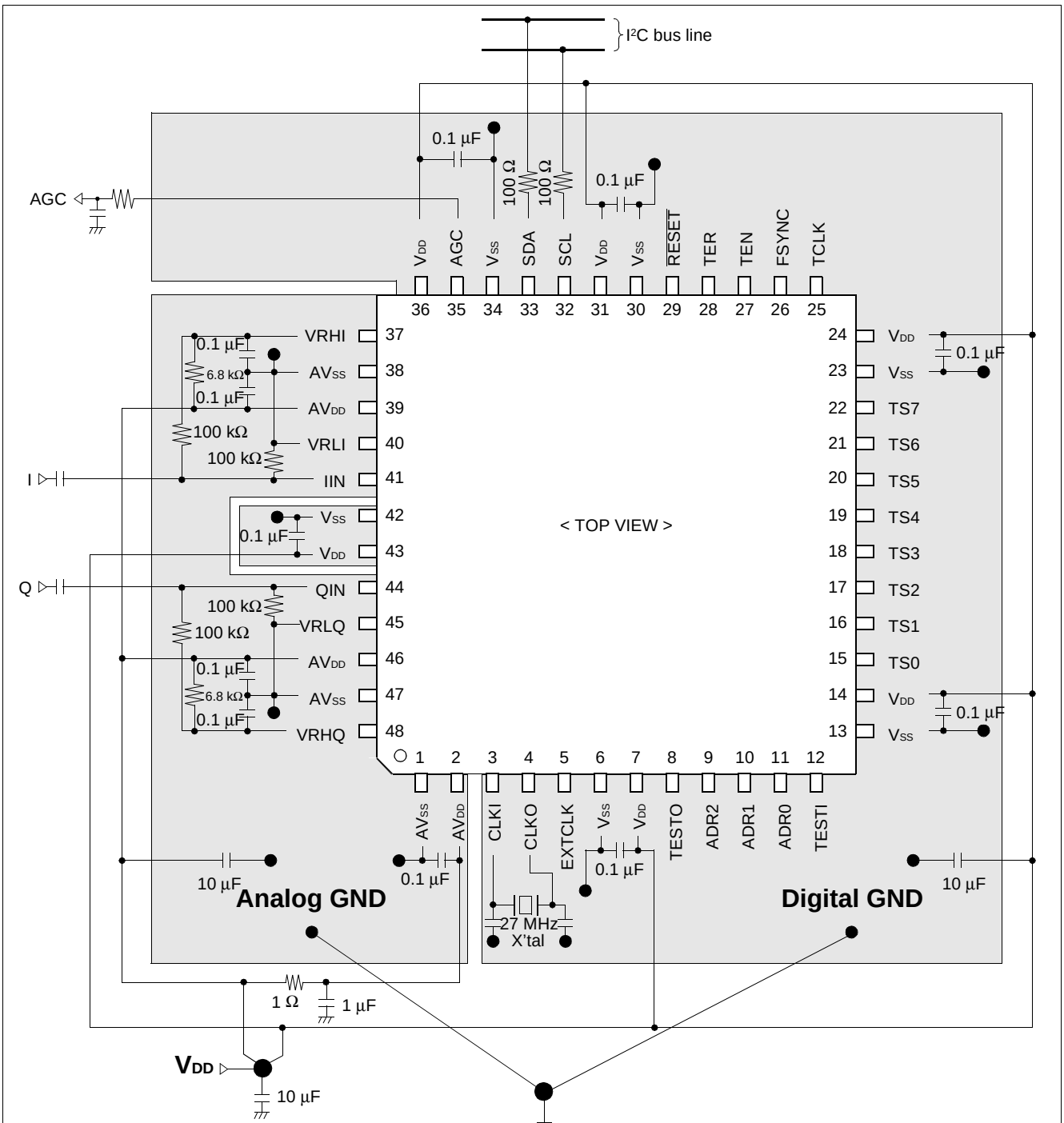


- When 27 MHz external clock is used.



MB86660A

■ PERIPHERAL CIRCUIT EXAMPLE



Notes: 1. The analog and digital power supplies should be separated and each GND pattern should be sufficient wide. Connect the bypass capacitors with good high frequency characteristics for V_{DD} – V_{SS} and AV_{DD} – AV_{SS}. Connect the analog and digital power supply pattern at a point such as the above illustration.

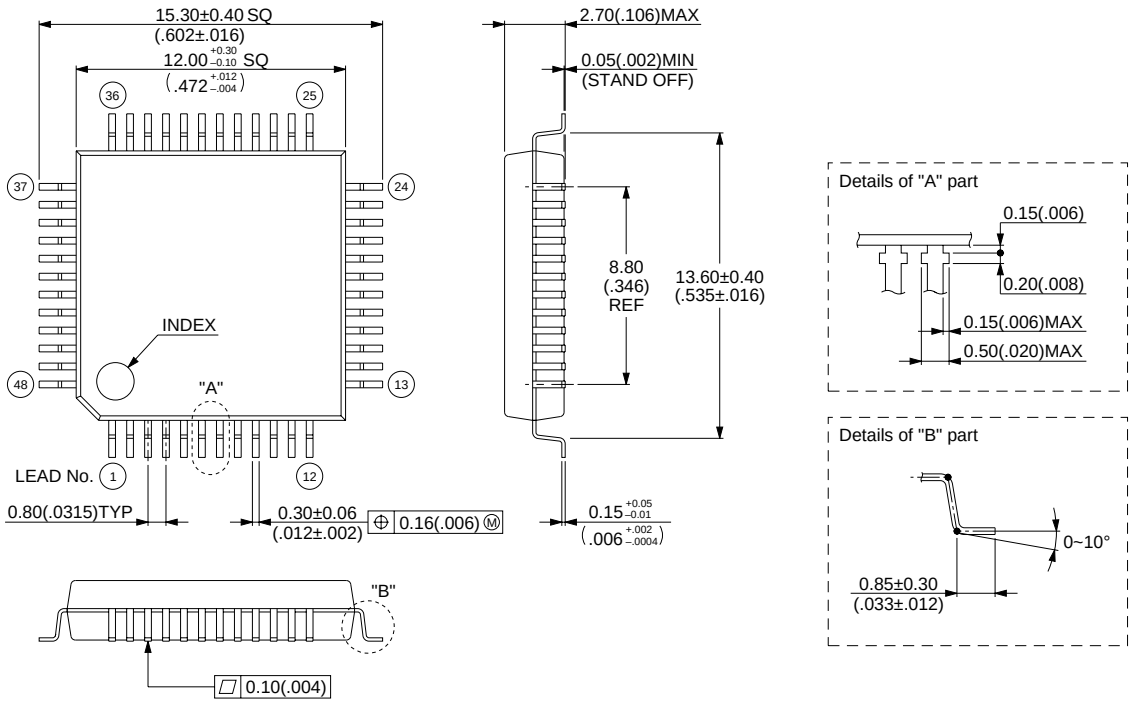
2. Connect the bypass capacitors with good high frequency characteristics between the analog GND 'AV_{SS}' and VRHI, VRLI, VRHQ and VRLQ which are the reference voltage of A/Ds. It is most important to stabilize the reference voltage for A/D. Furthermore, it is recommended to connect a large value of about 10 µF to AV_{SS}.

3. Use the board with 4-layer or more.

MB86660A

■ PACKAGE DIMENSION

48-pin plastic QFP
(FPT-48P-M15)



Dimensions in mm (inches)

MB86660A

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